Low Voltage Wizardry Provides the Ultimate Power-On Reset Circuit

by Bob Jurgilewicz

The Low Voltage Reset Problem

A fundamental problem plaguing most power supply supervisory ICs is the inability to establish the correct logic state at the reset node with low input supply voltages. Prior to power-up, external leakage currents often drive the reset node above the logic threshold of the microprocessor input. The LTC2903 (available in a 6-lead SOT-23) virtually eliminates this floating reset node problem by using a proprietary circuit to establish a low impedance path from the reset node to ground. Figure 1 shows just how easy it is to hook up a quad supervisor using the LTC2903.

When a supply, or supplies, resides below its supervisory threshold, the desired state at the reset node is logic low. Typically, an open-drain NMOS transistor is used to pull down the reset node (Figure 2). At low input voltages (<1V), the NMOS transistor lacks sufficient transconductance to overcome the pull-up current source, and the reset node may float up to a logic high level. If the reset node is signaling logic high while it is supposed to be low, a potential system reliability problem exists.

A common approach used to overcome the floating reset node is to integrate an active PMOS transistor pull-up and to specify an external resistor to ground. The external resistor pulls down the reset node at low input voltages. There are several drawbacks to this approach. First, unless an extra supply pin is dedicated to the internal PMOS source, the user has no control of the pull-up voltage (it is hard wired inside the chip). Second, there is a limit to how small the external resistor can be before the resistor overcomes the pull-up strength of the PMOS transistor. Third, low power systems will suffer while the reset node is logic high, since the external resistor will continuously dissipate power. With a 5V output and a 100kΩ external pull-down resistor, the system must support an additional 50µA load at the reset output, 2.5 times the typical quiescent current of most LTC voltage supervisors. Finally, a strong active pull-up makes wired-OR connections at the reset node impractical since an external circuit must overcome active pull-up current at logic low and guard against pushing reverse current into the pull-up supply at logic high.

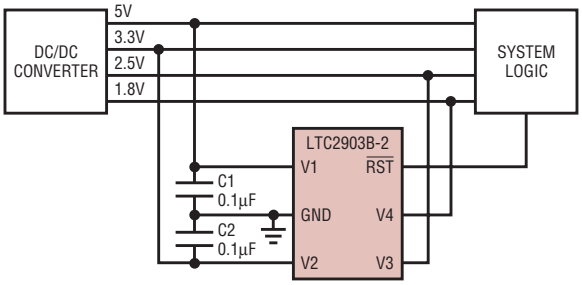

Figure 1. Typical application using the LTC2903B for quad supply monitoring

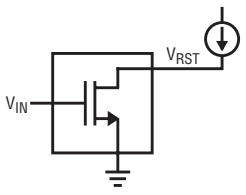

Figure 2. Traditional NMOS pull-down circuit

The Solution

The LTC2903 solves the floating reset node problem with none of the drawbacks discussed above. A proprietary circuit establishes, at low input voltages, a low impedance path from the reset node to ground. The low impedance path pulls down the reset node and will typically conduct current even when all input voltage supplies are at zero volts (see Figure 3). The reset output is guaranteed to sink at least 5 µA (V_{OL} = 0.15V) for V1, V2 or V3 down to 0.5V. Furthermore, the LTC2903 senses when there is sufficient voltage to operate the NMOS pull-down transistor reliably and will disconnect the low impedance shunt from the reset node. Removal of the low impedance shunt eliminates the leakage path that would interfere with any pull-up current source. The low impedance shunt re-enables when all supplies are below the level required for NMOS conduction.

A significant performance boost is obtained when input supplies are ramped together. Low impedance shunt action is available from three of the four inputs on the LTC2903 (V1, V2, V3), providing up to three times the pull-down strength available from just a single input. The LTC2923 Power Supply Tracking Controller provides such ramping capability (see waveforms in Figure 4). Figure 5 shows how the LTC2903 reset output performs against the competition with a 10kΩ resistor pulling up the reset node to

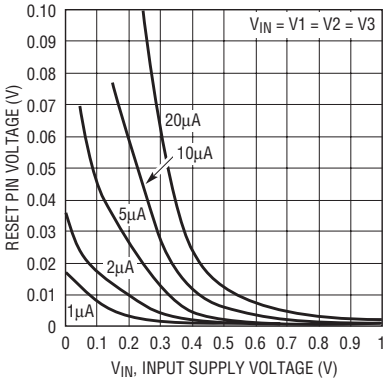

Figure 3. LTC2903 reset pin voltage (V_{OL}) vs external pull-up current at low input supply voltage

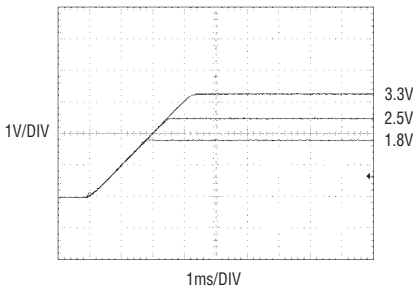

Figure 4. LTC2923 power supply tracking controller ramping example

the input supply. In particular, note that the reset output does not exceed 0.1V during power-on when ramping the supplies together (V1 = V2 = V3), which should satisfy the most demanding V_{OL} requirements.

LTC2903 Features

The LTC2903A, LTC2903B and LTC2903C is a family of quad supply monitors in 6-lead, low profile (1mm) SOT-23 packages. Table 1 summarizes available voltage input combinations. Threshold *accuracy* is ±1.5% of the monitored voltage over the temperature range of –40°C to +85°C (see "Implications of Threshold Accuracy" below).

Thresholds are configured for 10% undervoltage monitoring. For applications requiring an adjustable trip threshold, use the V4 input on the LTC2903A. Connect the tap point on an external resistive divider (R1, R2) placed between the positive voltage being sensed and ground, to the high impedance input on V4. The LTC2903A compares the voltage on the V4 pin to the internal 0.5V reference. Figure 7 demonstrates a generic setup for the positive adjustable application.

Table 1. LTC2903 voltage input combinations

LTC2903A	LTC2903B	LTC2903C
3.3V, 2.5V, 1.8V, ADJ (0.5V)	5V, 3.3V, 2.5V, 1.8V	5V, 3.3V, 1.8V, -5.2V

The reset output remains low during power-up, power-down and brownout conditions on any of the four voltage inputs. Voltage output low (V_{OL}) is guaranteed to be 150mV or less while pulling down 5µA with V1, V2 or V3 at 0.5V. A 200ms delay timer is integrated with the reset function. After all voltage inputs exceed their respective thresholds for 200ms, the reset output pulls high. The reset output style is open-drain with a weak internal pull-up to the V2 supply. External pull-up resistors can be used to improve rise times or to achieve logic levels above the V2 voltage.

Power supply glitch filtering is built in to each of the four comparators. The internal chip voltage (V_{CC}) is derived from the greater of the V1 or V2 inputs. Quiescent current drawn from V_{CC} is typically 20µA.

Implications of Threshold Accuracy

Specifying system voltage margin for worst-case operation requires consideration of three factors: power-supply tolerance, IC supply voltage tolerance and supervisor reset threshold accuracy. Highly accurate supervisors ease the design challenge by decreasing the overall voltage margin required for reliable system operation. Consider a 5V system with a ±10% power supply tolerance band. System ICs powered by this supply must operate reliably within this band (and a little more, as explained below). The bottom of the supply tolerance band, at 4.5V (5V–10%), is the exact voltage at which a *perfectly accurate* supervisor would generate a reset. Such a perfectly accurate supervisor does not exist—the actual reset threshold may vary over a specified band (±1.5% for the LTC2903 supervisors). Figure 6 shows the typical relative threshold accuracy for all four inputs, guaranteed over temperature.

With this variation of reset threshold in mind, the nominal reset threshold of the supervisor resides *below* the minimum supply voltage; just enough so that the reset threshold band and the power supply tolerance bands do not overlap. If the two bands overlap, the supervisor could generate a false or nuisance reset when the power supply remains within its specified tolerance band (say, at 4.6V).

Adding half of reset threshold accuracy spread (1.5%) to the ideal 10% thresholds, puts the LTC2903 thresholds at 11.5% (typical) below the nominal input voltage. For example, the 5V typical threshold is 4.425V, or 75mV below the ideal threshold of 4.5V. The guaranteed threshold lies in the band between 4.5V and 4.35V, over temperature.

The powered system must work reliably down to the lowest voltage in the threshold band, or risk malfunc-

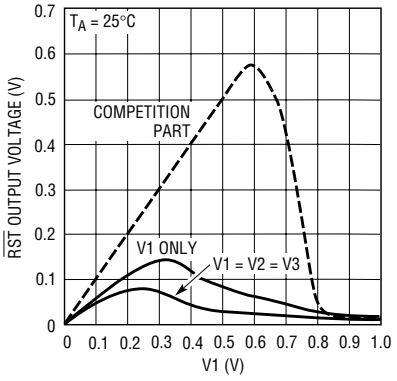

Figure 5. LTC2903 reset output voltage with a 10kΩ pull-up to V1 vs V1

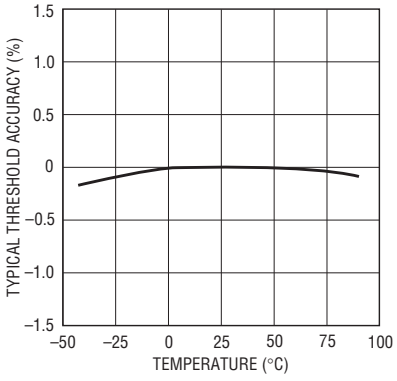

Figure 6. LTC2903 typical threshold accuracy vs temperature

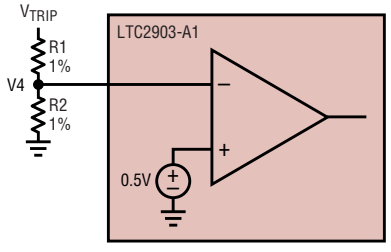

Figure 7. Setting the positive adjustable trip point

tion before the reset line falls. In our 5V example, using the 1.5% accurate supervisor, the system ICs must work down to 4.35V. System ICs working with a sloppier ±2.5% accurate supervisor must operate down to 4.25V, increasing the required system voltage margin, and the likelihood of system malfunction.

Noise Sensitivity

In any supervisory application, supply noise riding on the monitored DC voltage can cause spurious resets, particularly when the monitored voltage approaches the reset threshold. One common mitigation technique is to add hysteresis to the input comparator, but this has drawbacks. The amount of added hysteresis, usually specified as a percentage of the trip threshold, effectively degrades the advertised accuracy of the part. The LTC2903 does not use hysteresis.

To minimize spurious resets while maintaining threshold accuracy, the LTC2903 employs two forms of noise filtering. The first line of defense incorporates proprietary tailoring of the comparator transient response. Transient events receive electronic integration in the comparator and must exceed a certain magnitude and duration to cause the comparator to switch.

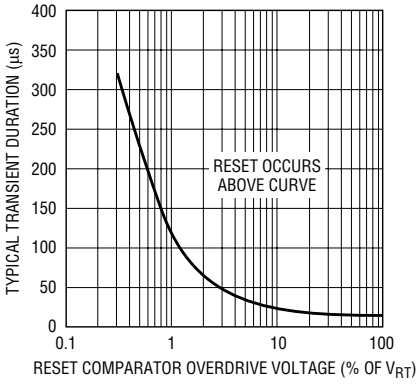

Figure 8. Typical transient duration vs overdrive required to trip comparator

Figure 8 illustrates the typical transient duration versus comparator overdrive (as a percentage of the trip threshold) required to trip the comparators. Once any comparator is switched, the reset line pulls low. The reset time-out counter starts once all inputs return above threshold, and the nominal reset delay time is 200 milliseconds. The counter clears whenever any input drops back below its threshold. This reset delay time effectively provides further filtering of the voltage inputs and is the second line of defense against noise. A noisy input with frequency components of sufficient magnitude above $f = 1/t_{RST}$ = 5Hz holds the reset line low, preventing oscillatory behavior on the reset line.

A reset line holding low provides a remarkably good indication of power supply problems. Common supply problems include improperly set output voltage and/or poor supply regulation.

Although all four comparators have built-in glitch filtering, use a bypass capacitor on the V1 and V2 inputs because the greater of V1 or V2 provides the V_{CC} for the part (a 0.1µF ceramic capacitor satisfies most applications). Apply filter capacitors on the V3 and V4 inputs if supply noise overcomes the built in filtering.

Conclusion

The LTC2903 quad supply monitor greatly improves system reliability by eliminating false resets and maintaining very high accuracy. Its proprietary reset pull-down circuit solves the long standing low voltage POR problem. The reset output can now maintain a logic-low at power-supply voltages down to zero volts. The reset output is guaranteed to sink at least 5µA (V_{OL} = 0.15V) for V1, V2 or V3 down to 0.5V. The LTC2903 monitors four voltages with 1.5% accuracy (over the entire temperature range) using comparators with built-in noise rejection. Non-standard voltages can be monitored with the 0.5V threshold adjustable input.

LT3468, continued from page 6

age dips on the supply powering the converter. In the end, the efficiency of the converter suffers which leads to longer charge times.

To illustrate this, two mid-range digital cameras from an industry-leading company are analyzed. Both camera photoflash units use a microprocessor controlled flyback converter. The first microprocessor controlled circuit is simple while the second uses numerous external components to implement a more complex control scheme. Table 3a shows a comparison of the performance parameters between the LT3468 circuit and the microprocessor-based circuits. More telling, though, is Table 3b, which makes the same comparison, but normalizes the input current.

The performance benefits of the LT3468 are obvious as shown in the nearly 44% reduction in charge time when compared to the microprocessor-based solutions. In addition to the charge time reduction, the LT3468 solution requires fewer, and smaller, components thus significantly reducing the overall size of the circuit.

Conclusion

The LT3468 and LT3468-1 provide a simple and efficient means to charge photoflash capacitors. The high levels of integration inside the parts result in tight output voltage distributions, small solution size, lower total solution cost and minimal microprocessor software overhead. When compared to traditional methods, charge times can be lowered by more than 44%. The LT3468 family offers a range of input currents for flexibility in the trade-off between input current and charge time.